## REMARKS

Reconsideration and allowance of the subject application are respectfully requested.

The Examiner objects to the specification noting a misspelling on page 4. This misspelling has been corrected. The Examiner also objects to the abstract requesting that the identification of Figure 5 be removed. The abstract has been revised. Withdrawal of the objection to the specification is respectfully requested.

The Examiner objects to claim 6 requesting that "wherein" be inserted. Features of claim 6 have been incorporated into claim 1. This objection is believed moot.

Claims 4, 5, 7, 8, and 11-14 stand rejected under 35 U.S.C. §112, second paragraph. This rejection is respectfully traversed.

Claims 4 and 11 have been amended to replace "and" with "or."

Regarding claims 5 and 12, Applicant disagrees that the word "adapt" is unclear. Both claims recite that the interface circuit, which includes the mapping circuit, is operable to "adapt" values and signal timings. The word "adapt," as used in this context, has a clearly understood and accepted meaning. For example, the Random House Dictionary defines adapt as "to adjust or become adjusted to new conditions, etc." The term adapted as used here is a "positive limitation" because it relates to some operation being performed, i.e., adapting signal values and timing in order to accommodate different value and timing properties of the memory. Withdrawal of this rejection is requested.

The Examiner contends that claims 7 and 14 do not limit their independent claims. Applicant disagrees. The independent claims recite at least one memory. Claims 7 and 14 recite a plurality of memories, each having a corresponding mapping circuit. Claims 7 and 14 exclude, for example, embodiments that have a single memory.

Claims 8, 11, 12 and 13 have been amended as requested by the Examiner.

Withdrawal of the rejections under 35 U.S.C. §112, second paragraph are respectfully requested.

Claims 1, 3, 4, 6, 8, 10, 11 and 13 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Publication US 2003/0167428 A1 to Gold. This rejection is respectfully traversed.

Claims 1 and 8 recite that the processor core, the memory, and the self-test controller are formed together on an integrated circuit. Although the Examiner refers to page 2, paragraph 16 of Gold, this paragraph discloses only that Gold's embedded testing memory method "is attractive for use in microprocessors." Gold neither discloses nor suggests that a processor core is a fabricated on the same integrated circuit as the components illustrated in Figure 2 of Gold. Figure 2 shows a built-in, self-test (BIST) engine 20, an address converter 24, and an embedded memory 28. There is no teaching in Gold that the BIST engine 20 corresponds to a processor core distinct from a self-test controller

Unlike Gold, the inventor recognized that a wide variety of possible component combinations on an integrated circuits comprising a memory, a self-test controller, and a

processor core make it particularly advantageous to have a generic, rather than a circuit-specific, self-test controller. Using the claimed mapping in this context enables different memory designs to be readily accommodated. The self-test circuit employs a test methodology based on physical memory addresses, which are readily converted by the mapping circuit to logical memory addresses appropriate for driving a particularly memory device.

Gold's goal is to use BIST technology to perform a pattern-sensitive test on a memory array that lacks a consist logical address and physical address mapping. Gold's teachings would not have motivated a person of ordinary skill in the art to adapt Gold's BIST circuit to incorporate a processor core on the same integrated circuit. Nor does Gold disclose or suggest that the address converter (mapping circuit) would enable a more generic, self-test controller to be used with a wide variety of different memory structures. To the contrary, Gold teaches adapting an existing BIST circuit to accommodate a particular memory structure in which the physical mapping and the logical mapping of the memory cell are not always consistent. See paragraph 5. Accordingly, the independent claims are not obviousness with respect to Gold, either alone or combination with U.S. Patent 6,469,945 to Patti et al.

The application is now in condition for allowance. An early notice to that effect is earnestly solicited.

Respectfully submitted,

**NIXON & VANDERHYE P.C.**

By: _____
John R. Lastova
Reg. No. 33,149

JRL:at
1100 North Glebe Road, 8th Floor
Arlington, VA 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100